AMENDMENTS TO THE CLAIMS

Claims 1-15 (Cancelled.)

16. (Original) A bipolar transistor formed on a wafer, the wafer having a buried layer and an epitaxial layer of a first conductivity type formed over the buried layer, the epitaxial layer having a top surface and a smaller dopant concentration than the buried layer, the transistor comprising:

an intrinsic base region of a second conductivity type formed on the epitaxial layer, the intrinsic base region including silicon and germanium, and having a first top surface and a vertically spaced-apart second top surface;

an isolation region formed on the first top surface of the intrinsic base region and over the second top surface of the intrinsic base region, the isolation region having a side wall;

an extrinsic emitter region formed on the isolation region and the intrinsic base region, the extrinsic emitter region having a side wall that is substantially aligned with the side wall of the isolation region; and

an intrinsic emitter region formed in the intrinsic base region, the intrinsic emitter region contacting the extrinsic emitter region.

17. (Original) The bipolar transistor of claim 16 wherein the intrinsic base region further includes carbon.

18. (Original) The bipolar transistor of claim 17 and further comprising an insulation region formed on the second top surface of the intrinsic base region, the insulation region having a top surface substantially coplanar with the first top surface.

19. (New) A bipolar transistor formed on a wafer, the wafer having a buried layer and an epitaxial layer of a first conductivity type formed over the buried

layer, the epitaxial layer having a top surface and a smaller dopant concentration than the buried layer, the transistor comprising:

a base region of a second conductivity type that contacts the top surface of the epitaxial layer, the base region having a top surface and including silicon and germanium;

an isolation region that contacts the top surface of the base region;

a first emitter region that contacts the isolation region and the base region; and

a second emitter region formed in the base region, the second emitter region contacting the first emitter region.

20. (New) The bipolar transistor of claim 19 wherein the base region has a first top surface and a vertically spaced-apart second top surface.

21. (New) The bipolar transistor of claim 20 wherein the first emitter region contacts the first top surface of the base region and is spaced apart from the second top surface of the base region.

22. (New) The bipolar transistor of claim 21 wherein the isolation region contacts the second top surface of the base region.

23. (New) The bipolar transistor of claim 22 wherein the isolation region has a substantially vertical side wall that lies over the second emitter region.

24. (New) The bipolar transistor of claim 23 wherein the first emitter region has a first substantially vertical side wall that contacts the vertical side wall of the isolation region.

25. (New) The bipolar transistor of claim 24 wherein the first emitter region has a second substantially vertical side wall that contacts the second emitter region and is spaced apart from the isolation region.

26. (New) The bipolar transistor of claim 25 and further comprising a layer of silicide that contacts the first top surface and the second top surface of the base region.

27. (New) The bipolar transistor of claim 26 wherein the base region includes a first section that has a first dopant concentration and a second section that includes a second dopant concentration that is heavier than the first dopant concentration.

28. (New) The bipolar transistor of claim 27 wherein the layer of silicide contacts the second section.

29. (New) The bipolar transistor of claim 28 and further comprising a non-conductive side wall spacer that contacts the second vertical side wall.

30. (New) The bipolar transistor of claim 20 wherein:

the isolation region has a substantially vertical side wall that lies over the second emitter region,

the first emitter region has a first substantially vertical side wall that contacts the vertical side wall of the isolation region; and

the first emitter region has a second substantially vertical side wall that contacts the second emitter region and is spaced apart from the isolation region.

31. (New) The bipolar transistor of claim 25 and further comprising a non-conductive side wall spacer that contacts the second vertical side wall.

32. (New) The bipolar transistor of claim 20 and further comprising a layer of silicide that contacts the first top surface and the second top surface of the base region.

33. (New) The bipolar transistor of claim 32 wherein:

the base region includes a first section that has a first dopant concentration and a second section that includes a second dopant concentration that is heavier than the first dopant concentration; and

the layer of silicide contacts the second section.